PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

AT

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G11B 7/14, 20/10

A1

(11) International Publication Number: WO 98/37555

(43) International Publication Date: 27 August 1998 (27.08.98)

(21) International Application Number: PCT/EP98/00984

(22) International Filing Date: 20 February 1998 (20.02.98)

(30) Priority Data:

08/804,105	20 February 1997 (20.02.97)	US
09/013,864	27 January 1998 (27.01.98)	US

(81) Designated States: CA, JP, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

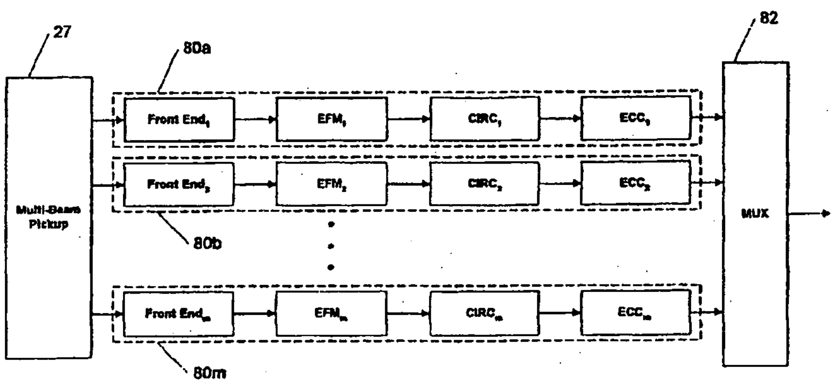
Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(71) Applicant: ZEN RESEARCH N.V. [NL/NL]; Van Engelenweg 21A, Curacao (AN).

(72) Inventors: ALON, Amir; 837 Duncardine Way, Sunnyvale, CA 94087 (US). FINKELSTEIN, Jacob; Hameyasdim Street 10B, 44219 Kfar Saba (IL). NAOR, Michael; Kaplan Hospital 11, 17600 Rehovot (IL).

(74) Agent: VOSSIUS & PARTNER; Siebertstrasse 4, D-81675 München (DE).

(54) Title: METHODS AND APPARATUS FOR CONCURRENTLY PROCESSING DATA FROM MULTIPLE TRACKS OF AN OPTICAL STORAGE MEDIUM



(57) Abstract

Methods and apparatus are provided for synchronously reading data from multiple tracks of an optical disk using multiple illumination beams. Circuitry is provided for use with a photodetector array to read and buffer data in parallel from the multiple adjacent tracks, while asynchronously providing processed data to a host processor. Circuitry is further provided for concurrently processing the signals read from the multiple data tracks to recover the data stored in the tracks.

METHODS AND APPARATUS FOR CONCURRENTLY PROCESSING DATA FROM MULTIPLE TRACKS OF AN OPTICAL STORAGE MEDIUM

Field of the Invention

This invention relates to methods and apparatus for retrieving information from an optical disk at high data rates by simultaneously and synchronously reading multiple adjacent tracks.

Background of the Invention

Due to their high storage density, long data retention life, and relatively low cost, optical disks are becoming increasingly popular as a means to distribute information. Large format disks have been developed for storing full length motion pictures. The compact disk (CD) format was developed and marketed for the distribution of musical recordings and has replaced vinyl records. High-capacity, read-only data storage media, such as CD-ROM and DVD, have become prevalent in the personal computer field, to the point that the DVD format may soon replace videotape as the distribution medium for video information.

An optical disk is made of a transparent disk or substrate in which data, in the form of a serial bit-stream, are encoded as a series of pits in a

1.6 µm, while DVD employs a track pitch only about one-half as wide.

Previously known methods of increasing the data transfer rate of optical disk readers have focused on increasing the rate at which the pits pass by the pickup assembly by increasing the rotational speed of the disk itself. Currently, drives with rotational speeds of up to 16× standard speed are commercially available, and even faster speeds have been achieved by moving to constant angular velocity designs. However higher disk rotational speeds place increasing demands on the optical and mechanical subsystems within the optical disk player, create greater vibration, and may make such players more difficult and expensive to design and manufacture.

Other previously known techniques for increasing average data transfer rates involve methods to intelligently anticipate future read requests by a host processor. It has been observed that data access by computers frequently exhibit "locality of reference," which means that a future data access will be local, in either space or time, to a previous data access. Thus a CD-ROM drive or controller can "read ahead" and buffer the data that the host processor is likely to request next. When the host processor next requests data from the optical disk drive, the drive first checks if the requested data have already been read and buffered. If the data have already been buffered, the drive simply sends the buffered data to the host, avoiding the delays associated with repositioning the pickup assembly and reading data from the optical disk itself. While such caching techniques may speed up average data access times, the maximum data transfer rate is still limited by the rotational

processed requires use of high performance devices to perform the functions at each of the stages in the processing chain.

The present application is directed to an improvement in the system described in the above-incorporated patent, wherein the multiplexer is moved to a later position in the processing chain, so that the plurality of data streams from multiple tracks on the disk may be demodulated, decoded, and error corrected before being multiplexed into a single data stream. Apparatus in accordance with the present invention may use a plurality of inexpensive, relatively low performance devices to perform the steps of demodulation, decoding, and error correction, while delivering throughput similar to that achieved by a high performance device performing these operations on a single multiplexed stream of data. Using the techniques of the present invention, it may be possible to construct a high performance system for processing the multiple data streams read from an optical disk, and which has a higher throughput than other similar systems, using standard low cost components.

It would therefore be desirable to provide apparatus and methods which permit simultaneous processing of data from multiple tracks in an optical disk reader.

It would also be desirable to provide demodulation, decoding, and error correction circuitry having higher throughput and at lower cost than previously known circuitry for processing the data from multiple tracks in an optical disk reader.

Brief Description of the Drawings

FIG. 1 is an illustrative block diagram of a previously known single beam optical disk reader;

FIG. 2 is an illustrative block diagram of a multi-beam optical disk reader;

FIG. 3 is a block diagram of a multi-beam optical disk reader built in accordance with the principles of the present invention;

FIG. 4 is a block diagram of the front end circuitry for extracting data from the signals output by the pickup assembly of FIG. 3;

FIGS. 5A, B, and C are block diagrams of the demodulator circuitry, decoder circuitry, and error correction circuitry, respectively, of the optical disk reader of FIG. 3;

FIGS. 6 and 7 are block diagrams of alternative embodiments of multi-beam optical disk readers built in accordance with the principles of the present invention; and

FIG. 8 is a block diagram of an alternate arrangement for the processing chain of an optical disk reader built in accordance with the principles of the present invention.

controller 24, the data signal is further processed by eight-to-fourteen (EFM) demodulation circuitry 17, Cross Interleaved Reed-Solomon Code (CIRC) decoding circuitry 18, error correction code (ECC) circuitry 19, and subcode circuitry 16. Controller 24 also controls focus and tracking circuitry 14, as well as buffer 20 and interface 22.

For a digital audio system, the data signals may be processed into suitable analog signals (using circuitry not shown) connected to audio means 21. Similarly, if the optical disk contains video images, the data signals may be processed for display on a TV or monitor. In computer applications the data signals are typically transferred from buffer 20 to host processor 23 via interface 22.

Spindle motor 11 spins optical disk 100 at a speed that depends upon the radial location of pickup assembly 12 (for example, for a 1× CD-ROM spindle speed, approximately 200-500 RPM), to maintain a constant linear velocity of an optical disk track relative to pickup assembly 12. For a CD-ROM format, this linear velocity is generally 1.4 m/s, while for the DVD format it approaches 4 m/s. Pickup assembly 12 typically includes a laser diode that illuminates only a single data track on optical disk 100 and an optical sensor onto which an image reflected from the optical disk is projected. The intensity, or other property, of the light beam reflected from the surface of optical disk 100 is modulated by inhomogeneities in the reflective surface of the optical disk (i.e., bumps or pits, referred to hereinafter as "data spots") arranged in spiral or circular tracks on optical disk 100.

Pickup assembly 12 includes circuitry to generate an electronic signal representative of the

Demodulated data words are also provided to subcode processor 16 which extracts data, such as block numbers, or song titles, that may be recorded in the subcode channels embedded in each block of data words.

For video and audio optical disk players, the data from CIRC decoder 18 represents, in digital form, the video or audio signal that was originally recorded and stored on the disk. These signals may then be converted to analog signals and the original recorded signal reproduced using conventional audio or video devices 21. Errors in the recovered audio or video signals are handled by interpolation and filtering circuitry (not shown) to calculate a value to use in place of the erroneous data. Because of the interpolation process, isolated errors in an audio or video signal are unlikely to be noticed when listening to the audio or viewing the video signals.

However, since a single bit error in data representing a computer program may render the program inoperable or the data unusable, optical disks used for the storage and distribution of data and programs must have very low data error rates. To reduce the data error rates to acceptably low levels, error correction codes (ECC) are added to the data when it is recorded to the disk. ECC circuitry 19 uses error correcting codes to detect and possibly correct errors in the data. Finally, the data are buffered in memory buffer 20 for transfer to host processor 23 via interface circuitry 22. Controller 24 coordinates operation of each of the optical disk reader subsystems and to control the operation of the optical disk reader as a whole.

Referring now to FIG. 2, an optical disk reader similar to that described in U.S. Patent Number

FIG. 1, except that multiple bit streams are processed concurrently, so additional circuitry is provided for buffering and synchronizing data transfers to subsequent processing circuitry. Front end circuitry 30 also includes a multiplexer for routing multiple data streams to demodulation circuitry 32 in the form of a single multiplexed data stream.

Demodulation circuitry 32, subcode circuitry 31, decoder circuitry 34, and error correction circuitry 36 of optical disk reader 25 are all similar in operation to their counterparts in optical disk reader 10 of FIG. 1. They differ principally in that they may be required to handle a much greater data throughput than similar circuitry used in single-beam optical disk reader 10.

Buffer memory 33 is provided to buffer the data read from the multiple data tracks, and to decouple the process of reading data from optical disk 100 from the process of transferring the data to host processor 37. Buffer 33 therefor is large enough to hold about as many data blocks from multiple data tracks of optical disk 100 as can be read in one revolution of optical disk 100. Controller 38 maps data from the multiple data tracks to memory 33 so that individual data blocks will be correctly assembled without overwriting one another. As will be appreciated by those of skill in the art of buffer design, this mapping may be either dynamic or static.

Description of the Present Invention

Referring to FIG. 3, multi-beam optical disk reader 40, constructed in accordance with the principles of the present invention is described. Multi-beam optical disk reader 40 is very similar to

titles, that may be recorded in the subcode channels embedded in each frame of data words.

Decoder circuitry 46 uses a form of Cross Interleaved Reed-Solomon Code, such as CIRC for CD-formats and PI PO structure for DVD, to decode the frames of data received in each of the data streams. The decoded frames are then assembled into sectors, which contain the data from multiple frames, and are made available to error correction circuitry 48 as multiple streams of sectors. Each sector contains a sector type identifier, used for determining which type of error correction or other processing to perform on the sector. Sectors also contain synchronization codes, data, and may contain error correction codes.

If the sector type identifier indicates that a sector contains error correction codes, error correction circuitry (ECC) 48 uses the error correction codes to detect and possibly correct errors in the data. The corrected data from each of the data streams is then made available to buffer memory 50 through multiplexer (MUX) 52. Buffer memory 50 uses MUX 52 to select one of the data streams, and transfers one sector of corrected data from ECC circuitry 48 to memory. Buffer memory 50 permits stored data to be transferred to host processor 23 via interface circuitry 22.

Controller 54 coordinates operation of each of the optical disk reader subsystems and controls the operation of the optical disk reader as a whole.

FIG. 4 shows a detailed view of front end circuitry 42, constructed using a separate PLL for each track. Multi-beam pickup assembly 27 outputs track data signals, $T_1 \ldots T_m$, corresponding to m tracks being

data words from one track into demodulated data words, or symbols, and assembles the symbols into frames. Additionally, demodulator units 60 may extract subcode data from the data stream, and send the subcode data to subcode processor 43.

For an 8× multi-beam CD-ROM reader, each demodulator unit 60 assembles 58,800 frames per second, each frame containing 32 bytes, for a total of approximately 1.9 million bytes per second. If the data from a seven beam, 8× system were combined into a single stream at the demodulator stage, the combined data stream would have a data rate of approximately 13.2 million bytes per second. Thus, applicant expects that retaining multiple data streams will permit use of a greater number of lower cost (slower) components.

FIG. 5B shows decoder circuitry 46, which comprises one single-track Cross Interleaved Reed-Solomon Code (CIRC) decoder unit 62 for each of the *m* data tracks being processed. Data from demodulator units 60 are sent into CIRC decoder units 62. Each of CIRC decoder units 62 decodes data from a single track, and assembles the data into sectors, which are sent to error correction circuitry 48.

For an 8× multi-beam CD-ROM reader, each CIRC decoder unit 62 assembles 600 sectors per second, each sector containing 2352 bytes, for a total of approximately 1.4 million bytes per second. If the data from a seven beam, 8× system were combined into a single stream at the decoder stage, the combined data stream would have a data rate of approximately 9.9 million bytes per second.

FIG. 5C shows error correction circuitry 48, which comprises one single-track error correction unit

data rate is highest, while using circuitry which processes a single data stream for later stages, such as decoding and error correction. Accordingly, in optical disk reader 60, Multiplexer 62 has been placed between demodulation circuitry 44 and decoder circuitry 34 in the processing chain. Multiplexer 62 combines the data from all of the single-track demodulation units of demodulation stage 44 into a single data stream. As shown in FIG. 6, multiplexer 62 sends the combined stream of data to buffer memory 50, where it is stored until the frames are requested by host 23, or are no longer needed. Alternatively, if later stages are capable of handling the throughput required to process the combined data stream, buffer memory 50 can be placed at the end of the processing chain, and the combined data stream from multiplexer 62 may be sent directly into decoder stage 34.

FIG. 7 shows another alternative embodiment, in which multiplexer 66 is located between decoder circuitry 46 and error correction circuitry 36 in the processing chain. Multiplexer 66 combines the data streams from the single-track decoder units in decoder stage 46 into a single data stream, which is stored in buffer memory 50. If the error correction stage is capable of handling the throughput required to process the combined data stream, buffer memory 50 may be placed at the end of the processing chain, after error correction stage 36.

FIG. 8 shows a yet further alternative arrangement of the processing chain for a multi-beam optical disk reader constructed in accordance with the principles of the present invention. The processing chain shown in FIG. 8 is arranged according to which beam is being processed, rather than according to

and modifications may be made without departing from the invention. It is intended in the appended claims to cover all such changes and modifications which fall within the true spirit and scope of the invention.

5. The apparatus as defined in claim 4, wherein the demodulation stage, decoding stage, and error correction stage are all part of the concurrent portion of the processing circuitry, the buffer is part of the serial portion of the processing circuitry, and the multiplexer is disposed between the error processing stage and the buffer.

6. The apparatus as defined in claim 4, wherein the demodulation stage is part of the concurrent portion of the processing circuitry, and the decoding stage, error correction stage, and buffer are part of the serial portion of the processing circuitry.

7. The apparatus as defined in claim 6, wherein the multiplexer is interposed between the demodulation stage, and the buffer.

8. The apparatus as defined in claim 6, wherein the multiplexer is interposed between the demodulation stage and the decoding stage.

9. The apparatus as defined in claim 4, wherein the demodulation stage and decoding stage are part of the concurrent portion of the processing circuitry, and the error correction stage and buffer are part of the serial portion of the processing circuitry.

10. The apparatus as defined in claim 9, wherein the multiplexer is interposed between the decoding stage and the buffer.

sampling the plurality of data signals to produce a plurality of digital data streams;

concurrently processing the plurality of digital data streams;

multiplexing the plurality of digital data streams into a single serial data stream; and

processing the serial data stream to produce the formatted data.

18. The method of claim 17, wherein the step of concurrently processing the plurality of digital data streams further comprises the steps of:

concurrently demodulating the plurality of digital data streams;

concurrently decoding the plurality of digital data streams; and

concurrently error correcting the plurality of digital data streams.

19. The method of claim 18, wherein the step of multiplexing the plurality of digital data streams follows the step of concurrently error correcting the plurality of digital data streams.

20. The method of claim 17, wherein the step of concurrently processing the plurality of digital data streams further comprises the step of concurrently demodulating the plurality of digital data streams, and the step of processing the serial data stream further comprises the steps of:

decoding the serial data stream; and

error correcting the serial data stream.

26. Apparatus for concurrently processing a plurality of streams of data simultaneously read from a plurality of tracks of an optical disk, the apparatus comprising:

a plurality of data stream processing circuits, each data stream processing circuit processing one of the plurality of data streams; and

a multiplexer for combining the outputs of the plurality of data stream processing circuits into a single data stream.

27. Apparatus as defined in claim 26, wherein each one of the plurality of data stream processing circuits comprises circuitry for demodulating a data stream.

28. Apparatus as defined in claim 27, wherein each one of the plurality of data stream processing circuits comprises circuitry for decoding a data stream.

29. Apparatus as defined in claim 28, wherein each one of the plurality of data stream processing circuits comprises circuitry for error correcting a data stream.

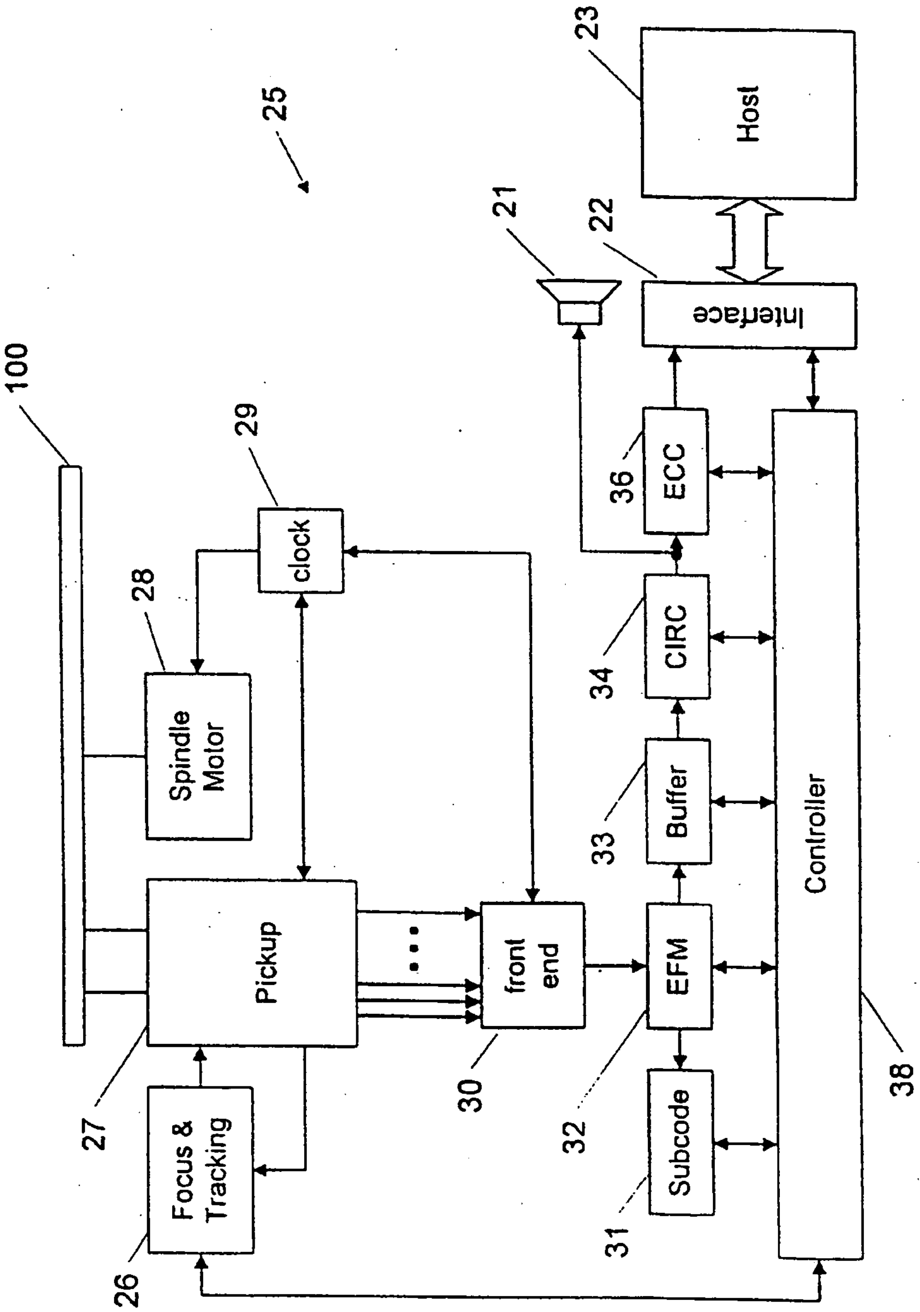

25
100
29
clock
28
Spindle Motor
Pickup
27
Focus & Tracking
26
front end
30
23
Host
21
22
Interface
ECC
36
CIRC
34
Buffer
33
EFM
32
Subcode
31
Controller
38

FIG. 2

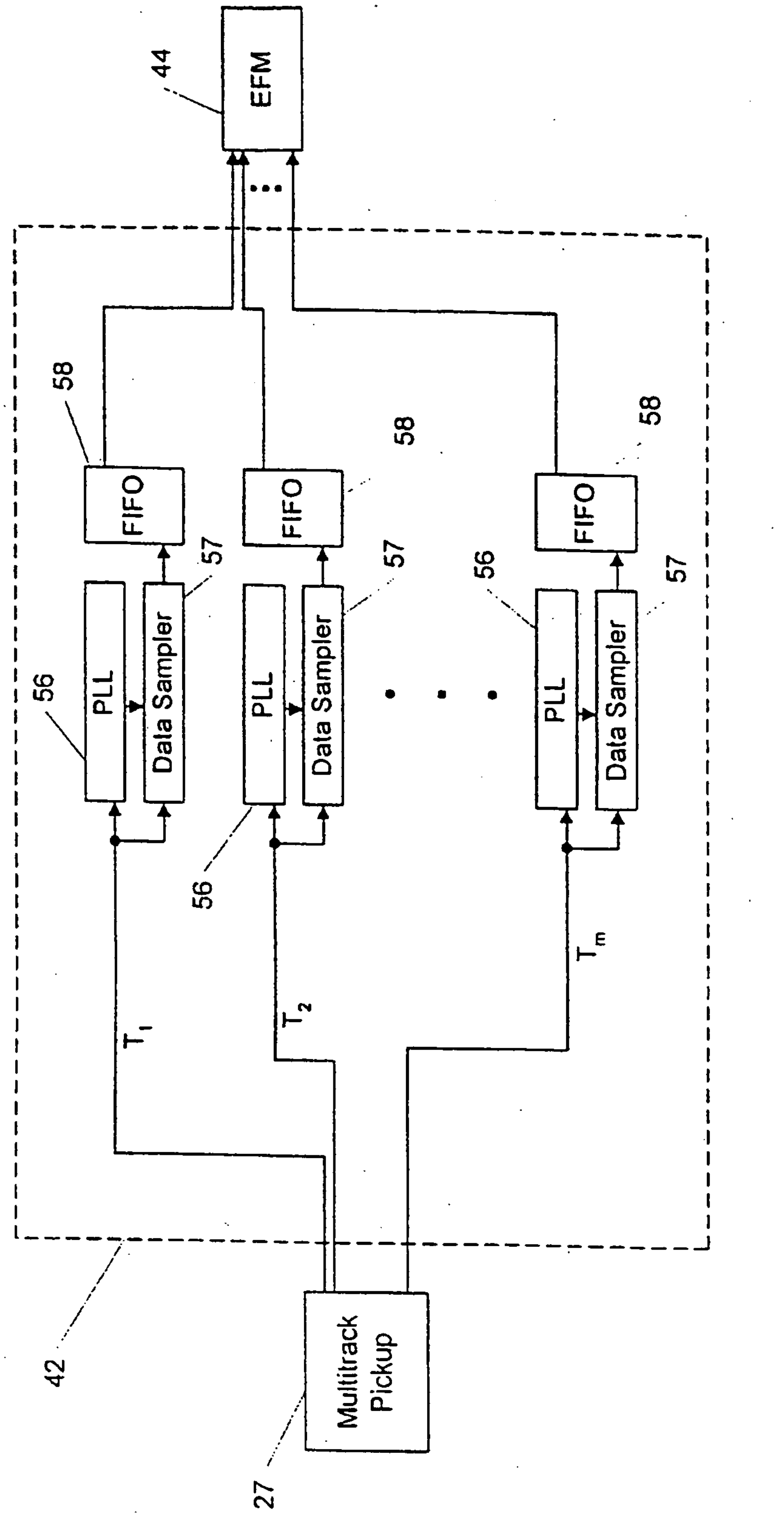

EFM
44
FIFO
58
PLL
Data Sampler
56
57
T_1
T_2
T_m
Multitrack Pickup
42
27

FIG. 4

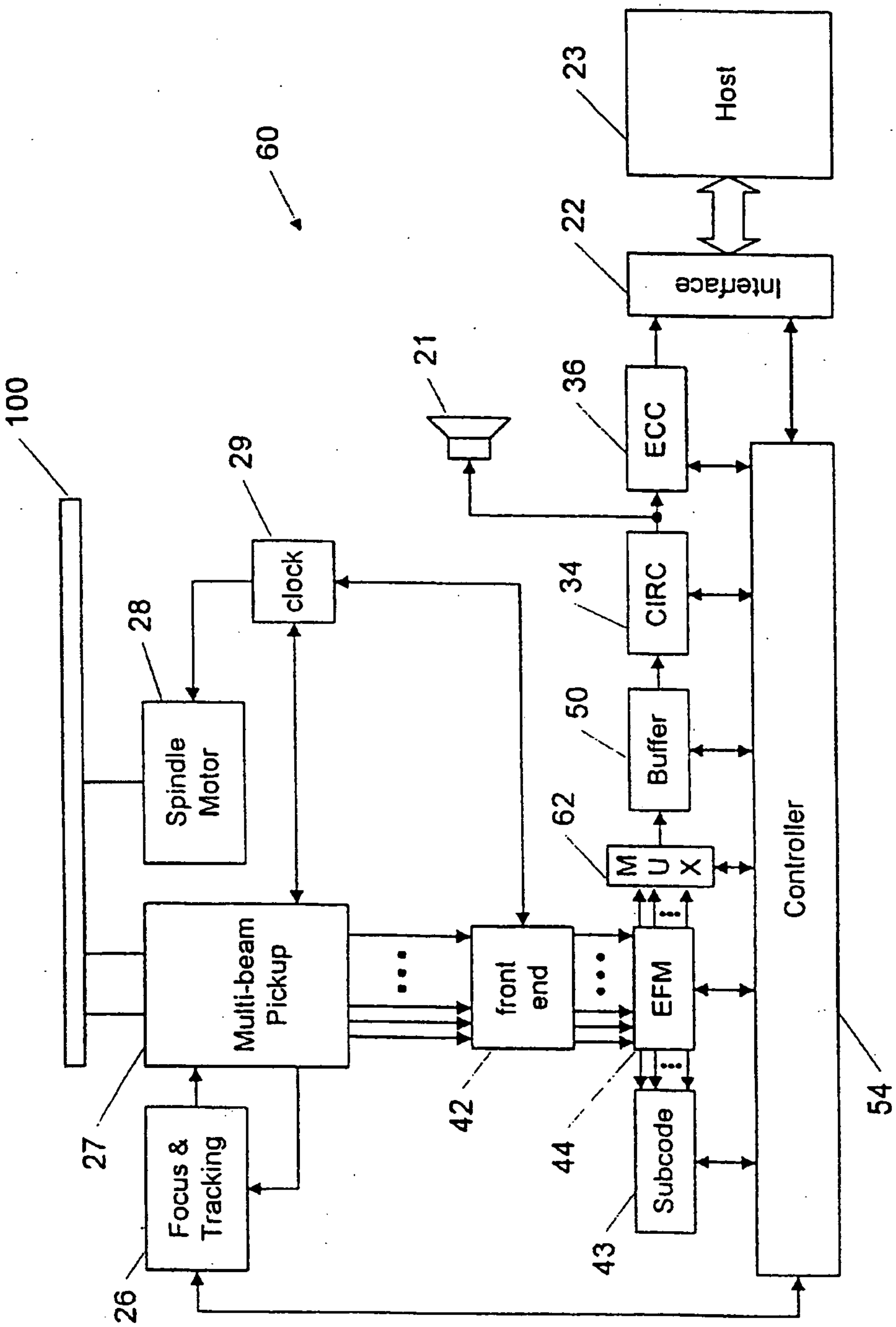

60
100
Spindle Motor
28
clock
29
Multi-beam Pickup
27
Focus & Tracking
26
front end
42
EFM
44
Subcode
43
MUX
62
Buffer
50
CIRC
34
ECC
36
21
Interface
22
Host
23
Controller
54

FIG. 6

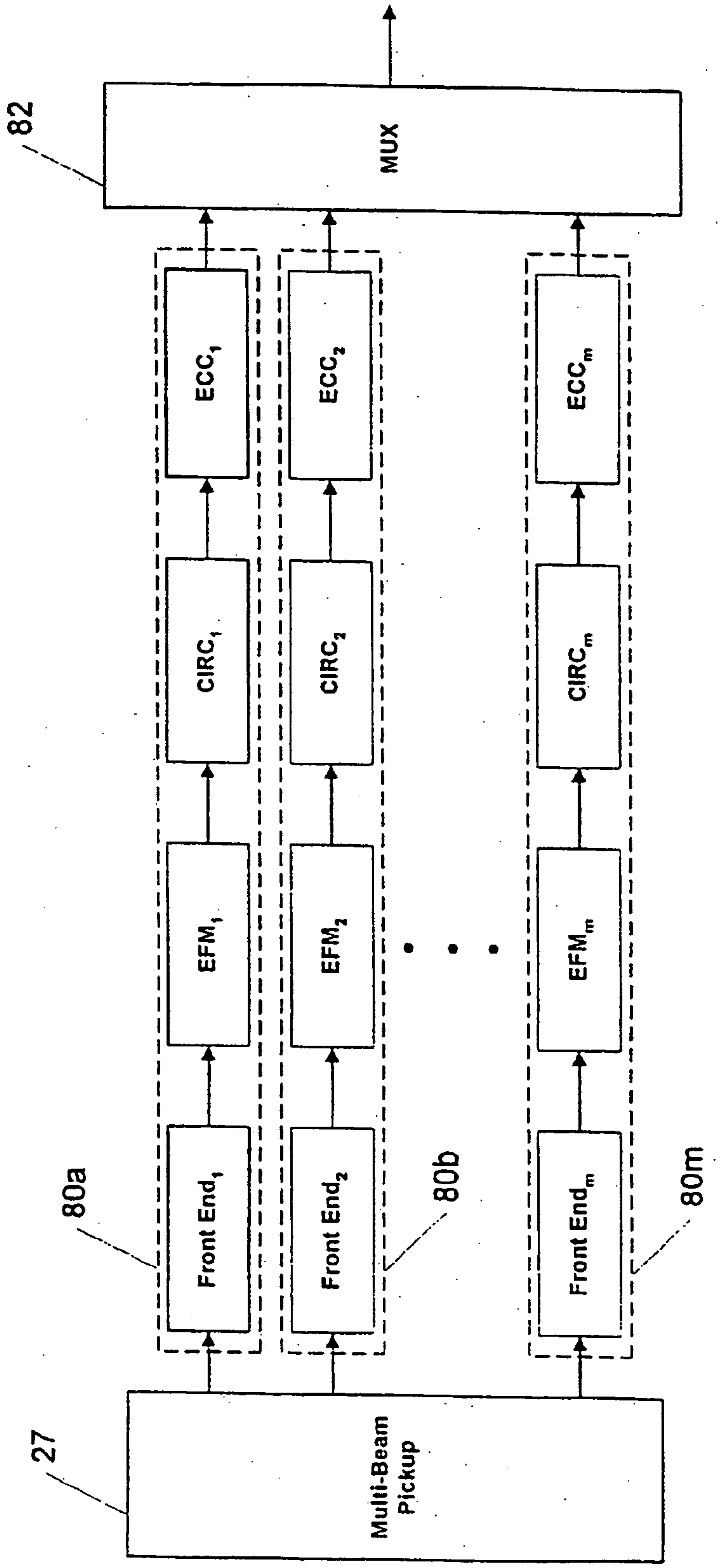

82
MUX
ECC_1
ECC_2
ECC_m
$CIRC_1$
$CIRC_2$
$CIRC_m$
EFM_1
EFM_2
EFM_m
Front End_1
Front End_2
Front End_m
80a
80b
80m
27
Multi-Beam Pickup

FIG. 8

INTERNATIONAL SEARCH REPORT

Inte ional Application No
PCT/EP 98/00984

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 714 096 A (SONY CORP) 29 May 1996 see abstract see column 3, line 18 - column 4, line 42; figures 1,2	16
X	EP 0 712 119 A (MATSUSHITA ELECTRIC IND CO LTD) 15 May 1996 see page 6, line 42 - page 7, line 5 see page 12, line 34 - line 55; figures 2,14	1,2,17, 26,27
A		3,15,18
X	EP 0 273 384 A (MATSUSHITA ELECTRIC IND CO LTD) 6 July 1988 see figure 7	1,2,12, 13,17, 24,26

1

Form PCT/ISA/210 (continuation of second sheet) (July 1992)